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Date: October 13, 2000

Docket No.: 630-1162P

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

This is a Request for filing a ☐ continuation ☒ divisional ☐ continuation-in-part application under 37 C.F.R. § 1.53(b) of pending prior Application No. 09/139,266 filed on August 25, 1998, the entire contents of which are hereby incorporated by reference,
by

Gyoung-Seon GIL

for

THIN FILM TRANSISTOR AND FABRICATION METHOD THEREFOR

1. ☒ Enclosed is an application consisting of specification, claims, declaration and drawings/photographs (if applicable).

2. ☒ The filing fee has been calculated as follows:

			LARGE ENTITY	SMALL ENTITY
	BASIC FEE		$710.00	$355.00
	NUMBER FILED	NUMBER EXTRA	RATE FEE	RATE FEE
TOTAL CLAIMS	6-20 =	0	x 18 = $0.00	x 9 = $0.00
INDEPENDENT CLAIMS	1-3 =	0	x 80 = $0.00	x 40 = $0.00
☐ MULTIPLE DEPENDENT CLAIMS PRESENTED			+ $270.00	+ $135.00
		TOTAL	$710.00	$0.00

3. ☒ A check in the amount of $710.00 to cover the filing fee and recording fee (if applicable) is enclosed.

4. ☐ Please charge Deposit Account No. 02-2448 in the amount of $0.00. A triplicate copy of this request is enclosed.

5. Amend the specification by inserting before the first line thereof the following:

a. ☒ --This application is a ☐ continuation ☒ divisional ☐ continuation-in-part of co-pending Application No. 09/139,266, filed on August 25, 1998, the entire contents of which are hereby incorporated by reference.--

b. ☐ --This application is a ☐ continuation ☐ divisional ☐ continuation-in-part of co-pending Application No. 09/139,266, filed on August 25, 1998. Application No. 09/139,266 is the national phase of PCT International Application No. PCT/_____/ filed on _____ under 35 U.S.C. § 371. The entire contents of each of the above-identified applications are hereby incorporated by reference.--

6. ☒ Enclosed is/are five (5) sheet(s) of formal drawings and/or photographs.

7. ☐ A statement claiming small entity status was filed in prior Application No. 09/139,266 on _____. See the attached copy of the statement claiming small entity status.

8. ☒ The prior application is assigned to Hyundai Electronics Industries Co.,Ltd.

9. ☒ A Preliminary Amendment is enclosed.

10a. ☒ Priority of Application No(s). 97-70069 filed in Korea on December 17, 1997 is/are claimed under 35 U.S.C. § 119. See attached copy of the Letter claiming priority filed in the prior application on August 25, 1998.

10b. ☐ Priority of International Appln. _____ filed on _____ under the Patent Cooperation Treaty and Application No. _____ filed in _____ on _____ under 35 U.S.C. § 119 are hereby reclaimed.

11. ☒ An Information Disclosure Statement and PTO-1449 form(s) are attached hereto for the Examiner's consideration.

12. ☒ Address all future communications to:

BIRCH, STEWART, KOLASCH & BIRCH, LLP
P.O. Box 747
Falls Church, VA 22040-0747
Telephone: (703) 205-8000

or

Customer No. 2292

13. ☐ An extension of time for _____( ) month(s) until _____ has been submitted in parent Application No. 09/139,266 in order to establish co-pendency with the present application.

14. ☐ Also enclosed herewith is the following:

_____

_____

_____

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By
Terry L. Clark, #32,644

P.O. Box 747
Falls Church, VA 22040-0747
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TLC:ewd
630-1162P

Attachments

(Rev. 09/29/2000)

PATENT
630-1162P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Gyoung-Seon GIL

Appl. No. New - Divisional Appl. of Appl. No. 09/139,266 Group: 2813

Filed: October 13, 2000 Examiner: L. Schillinger

For: THIN FILM TRANSISTOR AND FABRICATION METHOD THEREFOR

PRELIMINARY AMENDMENT

Assistant Commissioner
Washington, D.C. 20231

October 13, 2000

Dear Sir:

The following Preliminary Amendments and Remarks are respectfully submitted in conjunction with the above-identified application.

IN THE CLAIMS

Please cancel claims 7-14 without prejudice or disclaimer of the subject matter contained therein.

REMARKS

Claims 1-6 are pending in the present application. Claims 7-14 have been canceled. Claim 1 is in independent form.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly solicited.

In the event that any matters remain at issue in the application, the Examiner is invited to contact Terry L. Clark, Reg. No. 32,644 at (703) 205-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By: _____

Terry L. Clark
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TLC:ewd

THIN FILM TRANSISTOR AND FABRICATION METHOD THEREFOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, and more particularly to a thin film transistor and a fabrication method therefor applying a self-aligned process.

2. Description of the Conventional Art

In a conventional thin film transistor, when a gate electrode receives a voltage which is greater than a threshold voltage, and when a drain electrode receives a voltage greater than a source voltage, electrons, majority carriers in a source region, are migrated to a drain region via a channel region formed in a polysilicon layer, and thus a driving current is made to flow. However, when forming the channel region by applying the voltage to the gate electrode, the mobility of majority carriers is lowered due to a potential barrier formed by grain boundaries inside the polysilicon layer, and thus the driving current is reduced in a turn-on state.

Accordingly, there is provided an offset region of low resistance in the channel region at a side of the drain region in order to reduce the leakage current. A method of fabricating the conventional thin film transistor will now be described with reference to the appended drawings.

As shown in FIG. 1A, a polysilicon layer is deposited on an insulating substrate 1 by chemical vapor deposition (CVD), and patterned by a photo etching process, applying the polysilicon layer as a gate mask, for thus forming a gate

electrode 2.

As shown in FIG. 1B, a gate insulation film 3 is formed by depositing an insulating material on the surface of the insulating substrate 1 including the gate electrode 2, and an active layer 4 is deposited thereon by CVD.

A photoresist is applied on the active layer 4 and patterned by a photo etching process, for thus forming a photoresist pattern 5 as shown in FIG. 1C. Here, the photoresist pattern 5 defines channel and offset regions of the active layer 4.

As shown in FIGs. 1C and 1D, impurity regions 6a and 6b are formed by performing ion implantation, applying P or N-type impurities, into parts of the active layer 4 which are externally exposed, for thereby completing the fabrication of the conventional thin film transistor.

The impurity regions 6a and 6b define a source (a) and a drain (d), respectively, of a MOS transistor. In FIG. 1D, a, b, c, and d indicate the source, channel region, offset region, and drain, respectively.

However, a photomask process of the conventional method, which defines the length of each of the channel and offset regions, varies an offset current, which is dependent upon the degree of alignment, on a large scale, thereby reducing the reliability and reproducibility of the semiconductor device.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a thin film transistor and a fabrication method therefor capable of stabilizing an offset current which is dependent upon the degree of alignment by providing a self-aligned process, and thus improving properties of a semiconductor device.

To achieve the above objects, there is provided a thin film transistor which includes: a stepped substrate provided with a sidewall between upper portion and lower portions thereof; an active layer formed on the substrate; a gate insulation film on the active layer; a gate electrode formed on the gate insulation film corresponding to an upper part of the sidewall of the substrate; an insulation film formed on the gate insulation film between the gate electrode and the lower portion of the substrate; and impurity regions in the active layer corresponding to the upper and lower portions of the substrate.

In addition, to achieve the above objects, there is provided a fabrication method for a thin film transistor which includes the steps of: etching and patterning in order to form a sidewall between upper and lower portions thereof; forming an active layer on the substrate; forming a gate insulation film on the active layer; forming an insulation film on a first region of the sidewall and on the lower portion of the substrate, and forming a gate electrode on a second region of the sidewall and on the insulation film; and forming impurity regions in the active layer corresponding to the upper and lower portions of the substrate.

Additional advantages, objects and features of the invention will become more apparent from the description which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

FIGs. 1A-1D are vertical cross-sectional diagrams sequentially illustrating a conventional method of fabricating a thin film transistor;

FIG. 2 is a vertical cross-sectional view of a thin film transistor according to the present invention; and

FIGs. 3A-3H are vertical cross-sectional diagrams sequentially illustrating a method of fabricating the thin film transistor according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

With reference to the appended drawings, the thin film transistor according to the present invention and a fabrication method thereof will now be described.

FIG. 2 is a vertical cross-sectional view of a thin film transistor according to the present invention. As shown therein, a substrate 10 has a step formed on an upper surface thereof, and thus is provided with upper and lower portions 11, 12, and a sidewall 13 therebetween. An active layer 20 is formed on the upper and lower portions 11, 12, and on the sidewall 13. A gate insulation film 30 is formed on a part of the active layer 20 corresponding to the lower portion 12 and on a part of the active layer 20 corresponding to the sidewall 13. A gate electrode 42 is formed on the gate insulation film 30 corresponding to an upper part of the sidewall 13, and an insulation film 41 is formed on a part of the gate insulation film 30 corresponding to the lower portion 12 of the substrate 10 and on a part of the gate insulation film 30 corresponding to a lower part of the sidewall 13 of the substrate 10. Parts of the active layer 20, externally exposed on the upper and lower portions 11, 12 of the substrate 10, are respectively formed as impurity regions. In addition, an additional insulation film (not shown) is formed on the upper and lower portions 11, 12, and on

the sidewall 13.

The substrate 10 may be formed of an insulating material or an insulation film provided on a semiconductor material. The active layer 20 is a semiconductor film, and the insulation film 41 is formed of a spin-on-glass (SOG). Also, the active layer 20 is provided with a channel region (b) and an offset region (c) corresponding to the gate electrode 42 and insulation film 41, respectively.

FIGs. 3A-3H are vertical cross-sectional diagrams sequentially illustrating a method of fabricating the thin film transistor according to the present invention.

In FIG. 3A, the substrate 10 is etched and patterned, and thereby has the sidewall 13 provided between the upper and lower portions 11, 12 thereof. Here, the substrate 10 is formed of an insulating material or an insulation film which is provided on a semiconductor material, and an additional insulation film (not shown) is formed on the upper and lower portions 11, 12, and sidewall 13 of the substrate 10.

In FIG. 3B, the active layer 20 is deposited on the above described substrate 10 by CVD, and the gate insulation film 30 is formed on the active layer 20. Here, the active layer 20 is formed of a semiconductor film, and the gate insulation film 30 is formed by oxidizing the active layer 20, or by CVD.

The insulation film 41 formed of an SOG is deposited on the resultant structure, including the gate insulation film 30, as shown in FIG. 3C.

As shown in FIG. 3D, after an etch-back process, a part of the insulation film 41 remains on the gate insulation film 30 formed on the lower portion 12 of the substrate 10, being formed to the lower part of the sidewall 13 of the substrate 10.

In FIG. 3E, the gate electrode conductive film 42 is deposited on the resultant structure 10 including the gate insulation film 30 and insulation film 41. Here, doped

polysilicon is applied as the material of the gate electrode conductive film 42, and the lower part of the sidewall 13 of the substrate 10, corresponding to the insulation film 41, is defined as a first region, and the upper portion of the sidewall 13 of the substrate 10 corresponding to the gate electrode conductive film 42, is defined as a second region.

In FIG. 3F, an anisotropic etching process is applied to the gate electrode conductive film 42, thus forming the gate electrode 42, and a conductive sidewall formed to the gate insulation film 30 corresponding to the upper part of the sidewall 13 of the substrate 10.

As shown in FIG. 3G, the insulation film 41 is etched by utilizing the gate electrode 42 as an etching mask.

In FIG. 3H, by using the gate electrode 42 and insulation film 41 as a mask, ion implantation, applying As, P, etc., is performed into portions of the active layer 20 corresponding to the upper and lower portions 11, 12 of the substrate 10, for thus defining a source and a drain impurity regions of an NMOS transistor, or an ion implantation, applying B, BF_3, etc., is performed thereinto, for thus defining a source and a drain impurity regions of a PMOS transistor. By the above described method, the thin film transistor according to the present invention can be fabricated. Here, a, b, c and d in FIG. 3H indicate the source, channel region, offset region, and drain, respectively.

As described above, in the thin film transistor according to the present invention the impurity regions are formed by a self-aligned process, and the length of each of the channel and offset regions is defined in accordance with the thicknesses of each of the gate electrode and the insulation film, respectively, for thereby controlling the offset current to be more stabilized and accordingly for being

capable of improving the reliability and reproducibility of the semiconductor device.

Although the preferred embodiment of the present invention has been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as recited in the accompanying claims.

What is claimed is:

1. A thin film transistor, comprising:

a stepped substrate provided with a sidewall between upper and lower portions thereof;

an active layer formed on the stepped substrate;

a gate insulation film formed on the active layer;

a gate electrode formed on the gate insulation film corresponding to the sidewall of the substrate;

an insulation film formed on the gate insulation film between the gate electrode and the lower portion of the substrate; and

impurity regions in the active layer corresponding to the upper and lower portions of the substrate.

2. The thin film transistor of claim 1, wherein the stepped substrate is formed of an insulating material.

3. The thin film transistor of claim 1, wherein the insulation film is formed on the upper and lower portions, and on the sidewall of the substrate.

4. The thin film transistor of claim 1, wherein the active layer is a semiconductor film.

5. The thin film transistor of claim 1, wherein the insulation film is an SOG (spin-on-glass).

6. The thin film transistor of claim 1, wherein a portion of the active layer corresponding to the gate electrode is a channel region, and a portion thereof corresponding to the insulation film is an offset region.

7. A method of fabricating a thin film transistor, comprising the steps of:

etching and patterning a substrate in order to form a sidewall between upper and lower portions thereof;

forming an active layer on the substrate;

forming a gate insulation film on the active layer;

forming an insulation film on a first region of the sidewall and on the lower portion of the substrate, and forming a gate electrode on a second region of the sidewall and on the insulation film; and

forming impurity regions in the active layer corresponding to the upper and lower portions of the substrate.

8. The method of claim 7, wherein the substrate is an insulating material.

9. The method of claim 7, wherein the insulation film is formed on the upper and lower portions, and on the sidewall of the substrate.

10. The method of claim 7, wherein the active layer is a semiconductor film.

11. The method of claim 7, wherein the insulation film is an SOG (spin-on-glass).

12. The method of claim 7, wherein a portion of the active layer corresponding to the gate electrode is a channel region, and a portion thereof corresponding to the insulation film is an offset region.

13. The method of claim 7, wherein the step of forming the gate electrode and insulation film comprises the sub-steps of:

forming the insulation film on the lower portion of the substrate;

forming a conductive film on the upper portion and on the sidewall of the substrate, and on the insulation film;

forming a conductive sidewall on the sidewall of the substrate by applying an anisotropic etching process to the conductive film; and

etching the insulation film by using the conductive side wall as an etching mask.

14. The method of claim 13, wherein the conductive film is a polysilicon layer.

ABSTRACT OF THE DISCLOSURE

A thin film transistor and a fabrication method therefor, which thin transistor includes: a stepped substrate provided with a sidewall between upper portion and lower portions thereof; an active layer formed on the substrate; a gate insulation film on the active layer; a gate electrode formed on the gate insulation film corresponding to an upper part of the sidewall of the substrate; an insulation film formed on a part of the gate insulation film between the gate electrode and the lower portion of the substrate; and impurity regions formed in the active layer corresponding to the upper and lower portions of the substrate. The impurity regions are formed by a self-aligned process using an additional mask, which controls the length of channel and offset regions in accordance with the thicknesses of the gate electrode and insulation film, respectively, for thus obtaining a more stabilized offset current and accordingly improving the reliability and reproducibility of the semiconductor device.

FIG. 1A
CONVENTIONAL ART

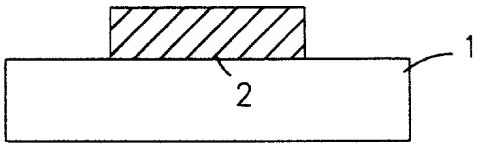


FIG. 1B
CONVENTIONAL ART

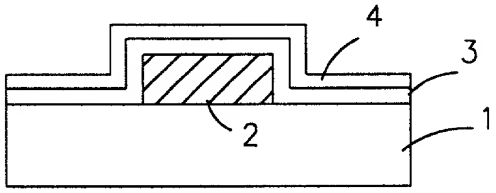


FIG. 1C
CONVENTIONAL ART

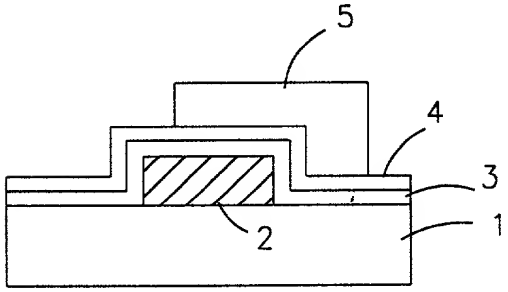


FIG. 1D
CONVENTIONAL ART

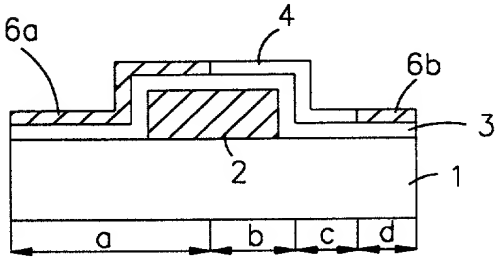


FIG.2

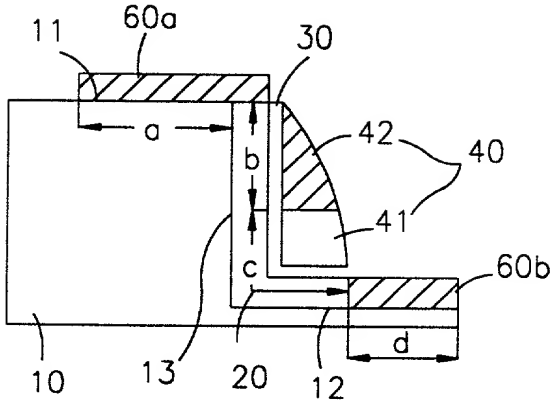


FIG.3A

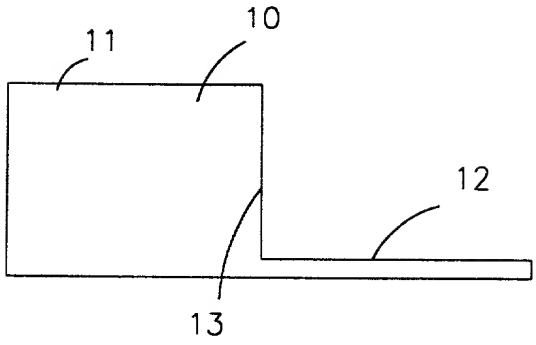


FIG.3B

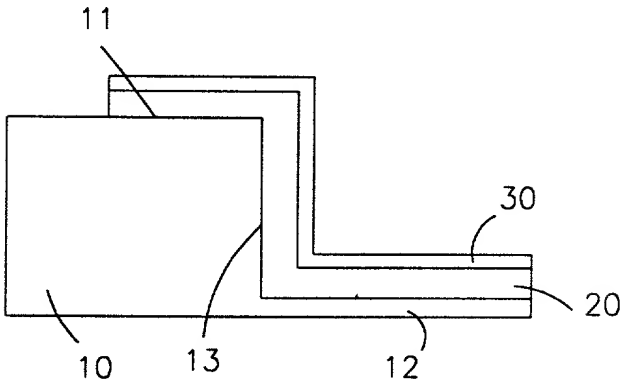


FIG.3C

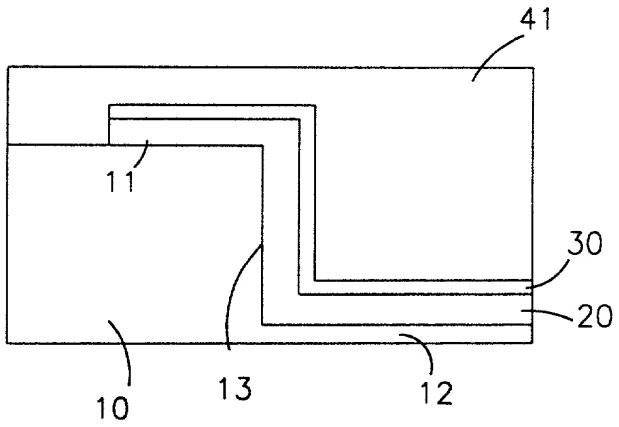


FIG.3D

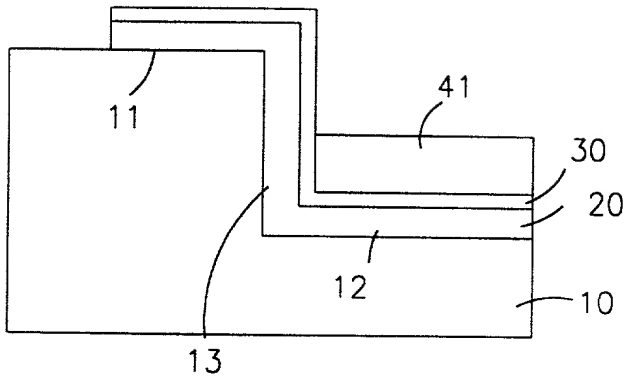


FIG.3E

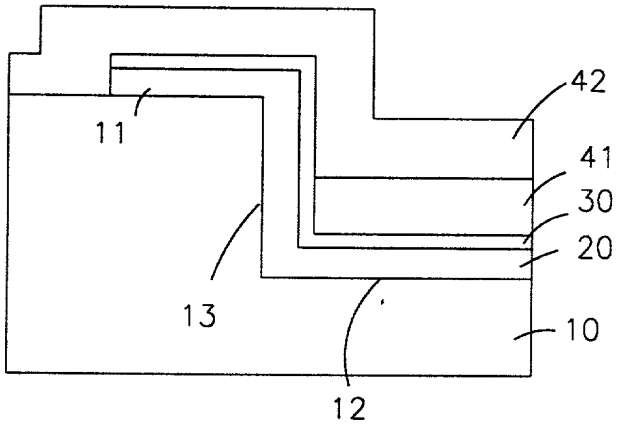


FIG.3F

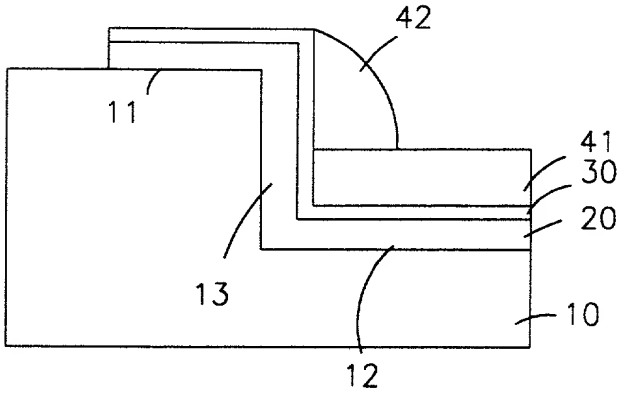


FIG.3G

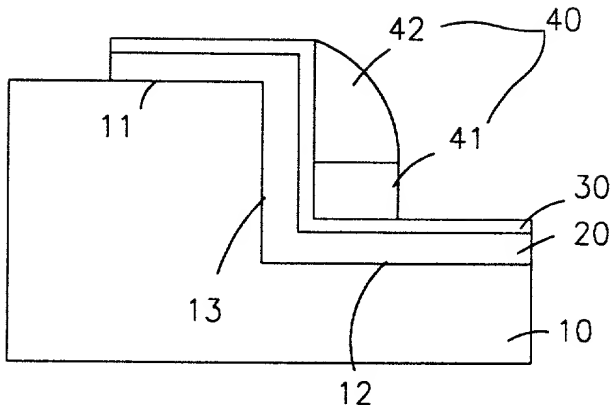
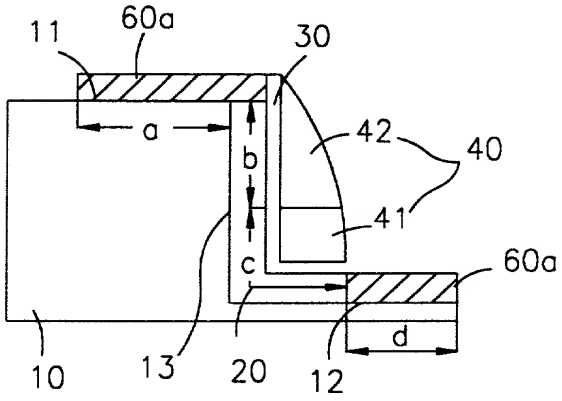


FIG.3H



BIRCH, STEWART, KOLASCH & BIRCH, LLP

COPY

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

COMBINED DECLARATION AND POWER OF ATTORNEY

FOR PATENT AND DESIGN APPLICATIONS

ATTORNEY DOCKET NO. 630-842P

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: ➡ THIN FILM TRANSISTOR AND FABRICATION METHOD THEREFOR

Fill in Appropriate Information - For Use Without Specification Attached: ➡

the specification of which is attached hereto. If not attached hereto,

the specification was filed on _____ as

United States Application Number _____; and /or

the specification was filed on _____ as PCT

International Application Number _____; and was

amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority Information: (if appropriate) ➡

Prior Foreign Application(s)			Priority Claimed	
70069/1997 (Number)	Korea (Country)	12/17/1997 (Month/Day/Year Filed)	☒ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

Insert Provisional Application(s): (if any) ➡

(Application Number) _____ (Filing Date) _____

(Application Number) _____ (Filing Date) _____

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months (6 Months for Designs) Prior To The Filing Date of This Application:

Insert Requested Information: (if appropriate) ➡

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Insert Prior U.S. Application(s): (if any) ➡

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

630-842P

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

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PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole Inventor:
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